WEST Search History

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DATE: Tuesday, January 25, 2005

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☐	L1	(deep adj sleep) same power$4	130

END OF SEARCH HISTORY

L11: Entry 14 of 19 File: USPT May 29, 1979

DOCUMENT-IDENTIFIER: US 4156907 A
** See image for Certificate of Correction **
TITLE: Data communications subsystem

CLAIMS:

1. A data communications subsystem including a data communications processor, a data communications memory resource using an autonomous memory for autonomous configurations and main host system memory for non-autonomous configurations, and a basic control module which connects to remote peripheral units, said data communications subsystem operating in connection with a main host system having a main central processor and main memory, said data communications subsystem comprising:

(a) said data communications processor being initiated by said main host system and including:

(a1) a local internal memory for storage of data transfer routines;

(a2) a plurality of cluster-interface hubs, each of which hubs is connected to either:

(i) a plurality of adapter-cluster module controllers, or

(ii) said basic control module having a basic control interface unit and a plurality of front-end controllers;

(a3) means to initiate, stop or interrogate each of said plurality of front-end controllers in the subsystem;

(a4) means to assemble and convey, to a selected front-end controller, an address of specific instruction-commands regarding data-transfer operations;

(a5) means to sense any halt in the main host system and thereupon to operate the data communications subsystem in an autonomous self-running mode during such halt period wherein input messages from peripherals and output messages from the main system are stored on disk files, and wherein said output messages are transferred to their destinations even when the main system is off-line, and said input messages are transformed to the main system from disk files when the main system is on-line again;

(b) said autonomous memory having direct access said basic control interface unit, said autonomous memory storing control data and information data dedicated to data transfer operations for use of said front-end controllers;

(c) said basic control module including:

(c1) a basic control interface unit, under control of said data communications processor, providing means to connecting said main host memory in non-autonomous subsystem configurations or means connecting said autonomous memory in autonomous

L11: Entry 8 of 19 File: USPT Sep 19, 2000

DOCUMENT-IDENTIFIER: US 6122756 A
TITLE: High availability computer system and methods related thereto

Brief Summary Text (5):
One design technique is commonly referred to as "fault tolerant." A computer system employing this technique is designed to withstand a hard fault that could shut down another type of computer system. Such a design typically involves replicating hardware and software so an applications program is running simultaneously in multiple processors. In this way, if a hard fault occurs in one processor or subsystem, the application program running in the other processor(s)/subsystem(s) still provides an output. Thus, as to the user, the computer system has performed its designated task. In addition to multiple processors, a voting scheme can be implemented, whereby the outputs from the multiple processors are compared to determine the correct output.

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L11: Entry 4 of 19 File: USPT Nov 4, 2003

DOCUMENT-IDENTIFIER: US 6643771 B2
TITLE: Method for initializing and shutting down a computer system

Brief Summary Text (18):
Because each of the elemental servers has its power supply unit, any number of elemental servers can be set to run in a sectional computer subsystem of the multiprocessor system, and turning power on/off can be performed separately per sectional computer subsystem.

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L7: Entry 13 of 26 File: USPT May 26, 1998

DOCUMENT-IDENTIFIER: US 5756981 A
**** See image for Certificate of Correction ****
TITLE: Optical scanner for reading and decoding one- and-two-dimensional symbologies at variable depths of field including memory efficient high speed image processing means and high accuracy image analysis means

Detailed Description Text (368):
Normal mode is used when flash memory is being programmed and otherwise when power consumption is of little concern. In these situations, an external power source is usually available. CPU 5222 automatically senses presence of an external power source and switches to this mode. Image-grab mode is entered when trigger switching driver module 5224 indicates that the trigger has been pulled. All subsystems required for image acquisition are awaken upon activation of image grab mode, but communication components such as the hardware UART remains in power-down mode. Processing mode is entered after the image is acquired and transferred to SDRAM 5212. Then the frame grabber subsystem is placed in power-down mode to save power. CPU 5222 processes the image in the SDRAM which typically involves reading a barcode. During transfer mode, the CPU 5222 wakes the hardware UART and transfers data out through serial port 5214. Alternatively, the parallel port may be used for data transfer. Idle mode is entered when device 4900 is not in operation. CPU 5222 and all other power-consuming subsystems are placed in power-down or idle mode. When the trigger is pulled, the system mode is switched back to image grab mode.

Detailed Description Text (411):
The power control process is shown in FIG. 60 and it starts with step 5210 of FIG. 62. The device 4900 provides power management by inclusion of a power management and driver module 5248 under control of the CPU and operation of monitor software loaded in flash memory 5210. The reset period for normal mode is set in step 6220. Idle mode is set in step 6230 which powers down the CCD image acquisition subsystem, the illumination LEDs, and the laser diode. The idle mode also places the CPU into standby mode. Idle mode is kept until the trigger is pressed. The state of the trigger is tested in step 6240. Once the trigger is pressed execution of the process continues in step 6250. Pressing the trigger puts the device in image grab mode. In image grab mode the CPU returns to a ready state (wakeup), the CCD sensor 5250 and the image acquisition subsystem turn on, including illumination LEDs and laser diode. Once the image is grabbed, execution of the process continues in step 6260, which begins image processing mode. In response to an indication of processing mode, the CCD array is turned off to save power. When the device enters image transfer mode the image data is transferred to the host for analysis. Then the laser diode 4922 and LEDs 4924 are turned off. Processing continues in a loop until power is totally removed from device 4900.

L7: Entry 10 of 26 File: USPT Mar 7, 2000

DOCUMENT-IDENTIFIER: US 6035347 A
** See image for Certificate of Correction **
TITLE: Secure store implementation on common platform storage subsystem (CPSS) by storing write data in non-volatile buffer

Detailed Description Text (6):
In implementation of the above preferred embodiment, the NVS processor 48 can be a IBM PPC-403 processor and IBM VOYAGER memory controller which are supported on a Common Platform Storage Subsystem (CPSS), a subsystem used in IBM PowerPC.TM.. It will be appreciated that a single chip processor, such as Intel I960RP, Intel I960RD, etc., may be used without departure from the principles of the present invention. In a preferred embodiment, minimal additional hardware design is required, and further, an early power down warning hardware may be used to signal the processor that the power will be down so that an interrupt to the NVS processor is processed. The NVS processor 48 is supported by a backup power source, such as a capacitor or a capacitor bank (pool), when the power is down. Using a capacitor or capacitors in the capacitor pool instead of using a battery to support the processor, the cost is significantly reduced. The capacitor(s) are arranged to have sufficient power to allow the data stored in the NV-Buffer 50 to be placed in a secured space and the data or instructions stored in the cache memories to be placed in the secured space. In a preferred embodiment, the NV-Buffer is supported by a capacitor or a capacitor bank when the main power is down. The processor 48 then transfers data and instructions in its cache memories and data in the NV-Buffer 50 to the NVS memory 52 via a fast dump operation. The details regarding the fast dump operation when the main power is down are described later. In an alternative embodiment, the NV-Buffer is supported by a battery assembly or pool when the main power is down. The processor 48 then may transfer data and instructions in its cache memories to the NV-Buffer 50 whereby a fast dump operation by the processor 48 and a fast dump space (see later) of the NVS memory 52 is not needed. It will be appreciated to one skilled in the art that other secure means can be used to ensure that once the main power is down, data and instructions are safely stored in a fast but less-cost fashion.